INFO INSTITUTE OF ENGINEERING COIMBATORE

(Autonomous, Affiliated to Anna University, Chennai)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI DESIGN

CURRICULUM AND SYLLABI R-2026

M.E./M.Tech.Programme (Full-Time)

Applicable to the students admitted from the Academic year 2026– 2027

INFO INSTITUTE OF ENGINEERING, COIMBATORE-641107.

(An Autonomous Institution, Affiliated to Anna University, Chennai)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E –VLSI DESIGN

R-2026, CHOICE BASED CREDIT SYSTEM

ABBREVIATIONS

BS - Basic Science (Mathematics, Physics, Chemistry)	**L** -Laboratory Course
ES-Engineering Science (General (G), Programme Core (PC), Programme Elective (PE)	**T** -Theory
SD - Skill Development	**LIT** - Laboratory Integrated Theory
	PW -Project Work
SL - Self Learning	**TCP** -Total Contact Period(s)

DEPARTMENT VISION

To be a center of excellence in Electronics and Communication Engineering by producing competent, innovative, ethical, and research-oriented professionals capable of addressing technological and societal challenges through lifelong learning.

DEPARTMENT MISSION

M1: To impart quality education in Electronics and Communication Engineering through a strong foundation in engineering principles, modern tools, and emerging technologies.

M2: To provide a conducive learning environment with advanced laboratories, industry interaction, and research opportunities that foster technical competence, innovation, problem-solving, communication, and teamwork.

M3: To nurture socially responsible and ethically committed engineers with leadership qualities, an entrepreneurial mindset, and a commitment to sustainable societal development.

PROGRAM OUTCOMES (POs)

1. An ability to independently carry out research /investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
2. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PROGRAM SPECIFIC OUTCOMES (PSOs)

1. Ability to design and implement innovative solutions to solve complex problems in VLSI.
3. Competence to independently undertake research projects involving simulation, measurement, and product development in VLSI-related fields.

Curriculum for I to IV Semester

Semester – I

S. No.	Course Code	Course Name	Course Type	Periods / Week		Credits	Category
				L-T- P	TCP		
1	26VL101T	Graph Theory and Optimization Techniques	T	3-1-0	4	4	BS
2	26VL102I	ASIC and FPGA Design	LIT	3-0-2	5	4	ES (PC)
3	26VLC03T	Digital CMOS VLSI Design	T	3-0-0	3	3	ES (PC)
4	26VLC04T	Advanced Digital System Design	T	3-1-0	4	4	ES (PC)
5	26VLC05T	Analog Integrated Circuit Design	T	3-0-0	3	3	ES (PC)
6	26VL106S	Technical Seminar	-	0-0-2	2	1	SD
Laboratory Courses							
7	26VL107L	Analog IC Design Laboratory	T	0-0-4	4	2	ES (PC)
			Total Credits		**25**	**21**	

Semester – II

S. No.	Course Code	Course Name	Course Type	Periods /Week		Credits	Category
				L-T- P	TCP		
1	26VL201T	Multi-Core Architecture and ISA Verification	T	3-0-0	3	3	ES (PC)

2	26VL202T	Data Converters IC Design	T	3-0-0	3	3	ES (PC)
3	26VL203T	VLSI testing and verification using UVM	T	3-0-0	3	3	ES (PC)
4	26VL$XXT	Programme Elective I	T	3-0-0	3	3	ES (PE)
5	26VL204T	Low Power VLSI Design	T	3-0-0	3	3	ES (PC)
6	26VL$NXL	Industry Oriented Course I	T	1-0-0	1	1	SD
7	26VL205N	Industrial Training	-	-	-	2	SD
8	-	Self-Learning Course	-	-	-	-	SL
Laboratory							
9	26VL206L	Verification using UVM Laboratory	L	0-0-4	4	2	ES(PC)
			Total Credits		**20**	**20**	

Semester – III							
S. No.	**Course Code**	**Course Name**	**Course Type**	**Periods /Week**		**Credits**	**Category**
				L-T- P	**TCP**		
1	26VL$XXT	Programme Elective II	T	3-0-0	3	3	ES (PE)
2	26VL$XXT	Programme Elective III	T	3-0-0	3	3	ES (PE)
3	26VL$XXT	Programme Elective IV	T	3-0-0	3	3	ES (PE)
4	26VL$XXT	Programme Elective V	T	3-0-0	3	3	ES (PE)
5	26VL$NXL	Industry Oriented Course I	-	1-0-0	1	1	SD
6	26VL301P	Project Work I	PW	0-0-8	12	6	SD
			Total Credits		**25**	**19**	

Semester – IV							
S. No.	Course Code	Course Name	Course Type	Periods /Week		Credits	Category
				L-T- P	TCP		
1	26VL401P	Project Work II	PW	0-0-24	24	12	SD
			Total Credits		24	12	

Total Credits = 72

PROGRAMME ELECTIVE COURSES – STREAMS

S. No.	Course Code	Course Name	Course Type	Periods / Week		Credits	Category
				L-T-P	TCP		
1	26VL$01T	VLSI Signal Processing	T	3-0-0	3	3	ES (PE)
2	26VL$02T	RF Integrated Circuit Design	T	3-0-0	3	3	ES (PE)
3	26VL$03T	Electromagnetic Interference and Compatibility	T	3-0-0	3	3	ES (PE)
4	26VL$04T	Physical Design of VLSI	T	3-0-0	3	3	ES (PE)
5	26VL$05T	Hardware / Software Co-Deign	T	3-0-0	3	3	ES (PE)
6	26VL$06T	CAD for VLSI Design	T	3-0-0	3	3	ES (PE)
7	26VL$07T	Nanotechnology	T	3-0-0	3	3	ES (PE)
8	26VL$08T	Pattern Recognition	T	3-0-0	3	3	ES (PE)
9	26VL$09T	Signal Integrity for High Speed Design	T	3-0-0	3	3	ES (PE)
10	26VL$10T	Network On Chip	T	3-0-0	3	3	ES (PE)
11	26VL$11T	VLSI for wireless Communication	T	3-0-0	3	3	ES (PE)

12	26VL$12T	DSP Structures for VLSI	T	3-0-0	3	3	ES (PE)
13	26VL$13T	Cryptography and Hardware Security in VLSI	T	3-0-0	3	3	ES (PE)
14	26VL$14T	Advanced Transistor Modelling	T	3-0-0	3	3	ES (PE)
15	26VL$15T	VLSI Architectures for Image Processing	T	3-0-0	3	3	ES (PE)
16	26VL$16T	Mixed Signal IC Design	T	3-0-0	3	3	ES (PE)
17	26VL$17T	Adaptive Signal Processing	T	3-0-0	3	3	ES (PE)
18	26VL$18T	Digital Image and Video Processing	T	3-0-0	3	3	ES (PE)
19	26VL$19T	Research Methodology	T	3-0-0	3	3	ES (PE)

Sl. No	Subject Area	Credits per Semester				Total Credits
		I	II	III	IV	
1	HUM	-	-	-	-	-
2	BS	4	-	-	-	4
3	ES(G)	-	-	-	-	-
	ES(PC)	16	14	-	-	30
	ES(PE)	-	3	12	-	15
	ES(ET)	-	-	-	-	-
4	SD	1	3	7	12	23
5	SL	-	-	-	-	-
6	OE	-	-	-	-	-
7	Non Credit (Mandatory) (✓Tick)	-	-	-	-	-
TOTAL		21	20	19	12	72



SEMESTER-I



26VL101T	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

To introduce the fundamental concepts of graph theory, graph algorithms, and their applications in solving connectivity, traversal, and network-related problems.

UNIT - I	BASIC CONCEPTS IN GRAPH THEORY	12 Hours

Graphs and graph models - Directed graph & undirected graph - Graph terminology and special types of graphs - Matrix representation of graphs and graph isomorphism - Connectivity- Euler and Hamilton paths -Trees - Spanning trees.

Activities: 1. Construct and analyze graph models using adjacency matrices.

2. Identify Euler, Hamilton paths, and spanning trees in graphs.

UNIT - II	GRAPH ALGORITHM	12 Hours

Search algorithms - Shortest path algorithms (Dijikstra's Algorithm) - Depth - First search on graph - Spanning tree algorithm - Theoretic algorithms - Performance of graph theoretic algorithms - Graph theoretic computer languages.

Activities: 1. Implement DFS and BFS on directed graphs.

2. Apply hardest path algorithms and analyze their performance.

UNIT - III	LINEAR PROGRAMMING	12 Hours

Formulation-Graphical solution :- Simplex method - Two-phase method – Big M – method – Transportation and Assignment Models.

Activities: 1. Formulate and solve LP problems using graphical and simplex methods.

2. Solve transportation and assignment problems with two-phase method.

UNIT - IV	NON-LINEAR PROGRAMMING	12 Hours

Constrained Problems - Equality constraints - Lagrangian Method, Inequality constraints - Karush, Kuhn - Tucker (KKT) conditions - Quadratic Programming - Wolfe's method.

Activities: 1.Solve constrained optimization using Lagrangian and KKT conditions.

2. Apply quadratic programming to non-linear optimization problems.

UNIT - V	SIMULATION MODEL AND NETWORK MODEL	12 Hours

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems - Project network - CPM and PERT networks – Critical path scheduling - Sequencing models.

Activities: 1.Perform Monte Carlo and discrete event simulations for queuing systems.

2. Construct CPM / PERT networks and apply critical path scheduling.

Total Hours	60

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%.

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Sharma, J. K. (Year of latest edition, e.g., 2023). Operations research: Theory & applications. Macmillan Publishers India.
2. Kapoor, V. K. (2023). Operations research (Rev. ed.). Sultan Chand &Sons.
3. Sharma,J.K.(2009).OperationResearch(3rded.).MacmillanPublishersIndiaLtd.
4. West,D.B.(2015).Introduction to graphtheory. Pearson Education.
5. Balakrishna, R., & Ranganathan, K. (2012). A textbook of graph theory. Springer Science and Business Media.
6. Rao, G. S. S. B. (2015). Discrete structures and graph theory. SciTech Publications Pvt. Limited.
7. Natarajan, A. M., Balasubramani, P., & Tamilarasi, A. (2014). Operations research. Pearson Education Pvt. Limited.

ONLINE RESOURCES:

1. https://onlinecourses.swayam2.ac.in/e-learning/preview/ntr26_ed100
2. https://onlinecourses.swayam2.ac.in/e-learning/preview/cec26_ma20
3. https://nptel.ac.in/courses/106106094
4. https://nptel.ac.in/courses/106104573

VIDEO REFERENCES:

1. https://youtube.com/playlist?list=PLEAYkSg4uSQ2fXcfrTGZdPuTmv98bnFY5
2. https://youtube.com/playlist?list=PLU6SqdYcYsfLV24T0XVb3z3mjl8QG0EBN

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Define the fundamental concepts, terminology, and types of graphs, including directed and undirected graphs.
CO2	Apply graph search algorithms, including Depth-First Search (DFS) and shortest path algorithms such as Dijkstra's algorithm, to solve graph-related problems.
CO3	Apply linear programming techniques to formulate mathematical models for real-world optimization problems.
CO4	Implement appropriate non-linear programming techniques to obtain optimal solutions for engineering and management optimization problems.
CO5	Assess project schedules using CPM and PERT networks to identify the critical path and support effective project planning.

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)					
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	-	-	-	-	-	-
CO2	3	3	-	3	3	-
CO3	3	3	-	2	2	-
CO4	-	-	-	-	-	-
CO5	3	3	-	3	2	-
Average	**1.8**	**1.8**	**-**	**1.6**	**1.4**	**-**

1.Low 2. Medium 3. High

26VL102I	ASIC AND FPGA DESIGN	L	T	P	C
		3	0	2	4

COURSE OBJECTIVES:

To Focus on Semi-Custom IC Design: Principles of Logic Cells, I/O Cells, Interconnect Architecture; Equal emphasis on FPGA & ASIC styles.

UNIT - I	INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN	15 Hours

Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell - Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors -Transistor Parasitic Capacitance- Logical Effort.

Practical Experiments:

1. Simulate CMOS inverter circuits and study transistor parasitic effects using a circuit simulator tool.
2. Running simulator and debug tools
3. Experiment with 2 state and 4 state data types

UNIT - II	PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC 1/0 CELLS	15 Hours

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx 1/0 blocks, ASIC Tool Flow.

Activity: Compare different programmable ASIC technologies (Anti-fuse vs SRAM vs EPROM) in terms of speed, power, and reconfigurability.

Practical Experiments:

1. Experiment with blocking and non-blocking assignments
2. Model and verify simple ALU
3. Model and verify an Instruction stack

UNIT - III	LOGIC SYNTHESIS, SIMULATION AND TESTING	15 Hours

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation - boundary scan test-fault simulation - automatic test pattern generation.

Activities:

1: Write simple Verilog/VHDL modules and synthesize them using logic synthesis tools.

2: Perform functional and timing simulations and create testbenches for boundary scan testing.

Practical Experiments:

1. Use an interface between testbench and DUT
2. Developing a test program
3. Create a simple and advanced OO testbench

UNIT - IV	ASIC PHYSICAL DESIGN	15 Hours

System partition -partitioning - partitioning methods - interconnect delay models and measurement of delay - floor planning - placement - Routing: global routing - detailed routing - special routing - circuit extraction – DRC

Activities:

1: Perform manual floor planning and placement for a simple ASIC design using CAD tools.

2: Analyze routing challenges and use tools to perform global and detailed routing; verify design rules compliance.

Practical Experiments:

Create a scoreboard using dynamic array .Use mailboxes for verification

UNIT - V	FPGA	15 Hours

FPGA Building Block Architecture- Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 FPGA Interconnect Routing Procedures.

Activities:

1: Explore and document the internal architecture of Xilinx XC4000 or Altera FLEX FPGA through data sheets.

2: Design and implement a simple combinational circuit on an FPGA development board and analyze routing.

Practical Experiments:

Generate constrained random test values

Using coverage with constrained random tests

Total Hours	75

Weightage: Continuous Assessment:50%,End Semester Examinations:60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

Smith, J. S. (2003). Application-specific integrated circuits. Pearson.

Smith, D. J. (1996). HDL chip design. Doone Publications.

Chan, K., & Mourad, S. (1994). Digital design using field programmable gate array. Prentice Hall.

Nekoogar, F. (1999). Timing verification of application-specific integrated circuits (ASICs). Prentice Hall PTR.

Wolf, W. (2004). FPGA-based system design. Prentice Hall PTR.

Kilts, S. (n.d.). Advanced FPGA design. Wiley Inter science.

ONLINE RECOURSES:

https://nptel.ac.in/courses/117106092

https://www.youtube.com/watch?v=oZSv68esbgI

https://www.youtube.com/watch?v=6ruLtdD5dUE

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Understand and Analyze ASIC Architectures & CMOS Logic Design.
CO2	Evaluate Programmable ASIC & FPGA Building Blocks
CO3	Model, Synthesize, and Test Digital Systems using HDLs.
CO4	Execute ASIC Physical Design Flow and Object-Oriented Verification

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	-	-	-	-	-
CO2	2	2	3	2	2
CO3	3	2	3	3	3
CO4	3	3	3	3	3
Average	2	1.7	2.25	2	2

26VLC03T	Digital CMOS VLSI Design	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

To Understand CMOS basics and design combinational/sequential circuits; apply structured VLSI design through case studies.

UNIT - I	MOS Transistors and CMOS Inverter	9 Hours

MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing.

Activities: 1. Simulate CMOS inverter characteristics and sizing effects
2. Draw stick diagrams and analyze power-delay trade

UNIT - II	CMOS, Combinational Circuits	9 Hours

Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS.

Activities: 1. Design combinational logic using different CMOS styles
2. Analyze power and switching activity in logic gates

UNIT - III	CMOS, Sequential Circuits	9 Hours

Latches vs registers, flip-flops, dynamic/static registers, clocking strategies, Schmitt trigger, mono/astable circuits.

Activities: 1. Implement various flip-flops and compare timing behavior
2. Design clocking schemes for latch/register pipelines

UNIT - IV	CMOS Sub System Design	9 Hours

Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements.

Activities: 1. Design fast adders and multipliers
2. Build and simulate small subsystems (e.g., counter + MUX)

UNIT - V	Performance Estimation & Design Techniques	9 Hours

Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design.

Activities: 1. Estimate delay and power for sample circuits
2. Compare synchronous vs self-timed circuit design

Total Hours	45

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

REFERENCES:

1. Weste, N. H. E., & Harris, D. (2011). CMOS VLSI design: A circuits and systems perspective. Pearson.
2. Rabaey, J. M., & Nikolić, B. (2003). Digital integrated circuits. Pearson.
3. Martin, K. (2011). Digital integrated circuit design. Oxford University Press.
4. Palnitkar, S. (2003). Verilog HDL (2nd ed.). Pearson Education.
5. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). Digital integrated circuits,Pearson.

ONLINE COURSES:

1. https://nptel.ac.in/courses/108106158
2. https://onlinecourses.nptel.ac.in/e-learning/preview/noc22_ee08

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain CMOS basics in digital circuits.
CO2	Analyze and design CMOS-based combinational and sequential circuits
CO3	Apply various CMOS logic styles and techniques to optimize digital subsystems
CO4	Evaluate and estimate circuit performance using structured approaches for subsystem design.

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	-	-	-	-	-
CO2	3	-	-	2	2
CO3	3	3	-	3	3
CO4	3	3	-	2	2
Average	2.25	1.5	-	1.75	1.75

1. Low 2. Medium 3. High

26VLC04T	Advanced Digital System Design	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

To study design and analysis of synchronous/asynchronous sequential circuits, PLD/ROM design, combinational/PLA testing, and Verilog HDL for digital system design.

UNIT - I	Sequential Circuit Design	12 Hours

State diagrams/tables, state assignment & reduction, synchronous circuit design, iterative circuits, ASM charts.

Activities: 1. Design state diagrams for given problems
2. Implement synchronous circuits using ASM

UNIT - II	Asynchronous Sequential Circuit Design	12 Hours

Flow table reduction, race conditions, hazards (static/dynamic/essential), mixed-mode circuits, vending machine controller design.

Activities: 1. Analyze and minimize flow tables
2. Identify and eliminate hazards

UNIT - III	Fault Diagnosis and Testability Algorithms	12 Hours

Fault table, path sensitization, Boolean difference, D & Kohavi algorithms, PLA faults, DFT, BIST techniques.

Activities: 1.Generate fault tables for combinational circuits
2. Simulate fault detection using D-algorithm

UNIT - IV	Synchronous Design Using Programmable Devices	12 Hours

PLD families, PLA/PAL-based circuit design, ROM design, FSM realization using PLDs, FPGA (Xilinx Vertex 7).

Activities: 1. Implement FSM using PLA/PAL
2. Program and simulate FSM on FPGA

UNIT - V	System Design Using Verilog	12 Hours

Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.

Activities: 1. Write and simulate Verilog code for registers, counters, serial adders
2. Design and test a simple microprocessor in Verilog

	Total Hours	60

Weightage: Continuous Assessment: 50%, End Semester Examinations: 50%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

REFERENCES:

1. Roth, C. H., Jr. (2013). Fundamentals of logic design (7th ed.). Thomson Learning.
2. Arnold, M. G. (1999). Verilog digital – computer design. Prentice Hall PTR.
3. Biswas, N. N. (2001). Logic design theory. Prentice Hall of India.
4. Lala, P. K. (2020). Fault tolerant and fault testable hardware design. B S Publications.
5. Lala, P. K. (2015). Digital system design using PLD (Reprint ed.). B S Publications.
6. Palnitkar, S. (2003). Verilog HDL – A guide to digital design and synthesis. Pearson.

ONLINE RESOURCES:

1. https://nptel.ac.in/courses/117106114
2. https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain the fundamentals of synchronous and asynchronous sequential circuits
CO2	Analyze and design sequential circuits using state diagrams and ASM charts.
CO3	Apply fault diagnosis and testability algorithms to digital circuits
CO4	Develop and simulate digital systems using Verilog HDL and FPGA.

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	-	-	-	-	-
CO2	3	-	-	2	2
CO3	3	3	-	3	3
CO4	3	3	-	2	2
Average	2.25	1.5	-	1.75	1.75

1. Low **2. Medium** **3. High**

26VLC05T	Analog Integrated Circuit Design	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

To Study single-stage amplifier design, high-frequency/noise characteristics, operational amplifiers, voltage/current reference circuits with practical exercises.

UNIT - I	Single Stage Amplifiers	9 Hours

MOS physics, equivalent circuits, CS, CG, source follower, differential & cascode amplifiers, design for SR, gain, BW, ICMR, power, voltage swing.

Activities: 1. Design and simulate CS, CG amplifiers
2. Calculate gain, bandwidth, slew rate for given specification

UNIT - II	High Frequency and Noise Characteristics of Amplifiers	9 Hours

Miller effect, pole analysis, frequency response of stages, noise sources, noise analysis in single stage and differential amplifiers.

Activities: 1. Analyze frequency response using pole-zero plots
2. Simulate noise performance in amplifiers.

UNIT - III	Negative Feedback Amplifiers and Operational Amplifiers	9 Hours

Feedback types, loading effects, op-amp parameters, one/two-stage op-amps, gain boosting, slew rate, PSRR, noise in op-amps.

Activities: 1.Design and simulate negative feedback circuits
2. Evaluate gain, slew rate, and PSRR of op-amps

UNIT - IV	Stability and Frequency Compensation of Two Stage Operational Amplifier	9 Hours

Twostage op-amp analysis, phase margin, compensation methods, slew rate issues, advanced compensation techniques.

Activities: 1. Analyze phase margin and stability in two-stage op-amps
2. Implement frequency compensation methods in simulations

UNIT - V	Voltage and Current References	9 Hours

Current mirrors (Wilson, Widlar, Cascode), high swing cascode sinks, supply/temperature independent biasing, PTAT & CTAT currents, constant-Gm biasing.

Activities: 1. Design and simulate various current mirrors
2. Implement PTAT and CTAT current references

Total Hours	45

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

REFERENCES :

1. Razavi, B. (2016). Design of analog CMOS integrated circuits (2nd ed.). Tata McGraw Hill.
2. Sansen, W. M. C. (2007). Analog design essentials. Springer.
3. Grebene, A. B. (2003). Bipolar and MOS analog integrated circuit design. John Wiley & Sons, Inc.
4. Allen, P. E., & Holberg, D. R. (2013). CMOS analog circuit design (3rd ed.). Oxford University Press.
5. Natarajan, A. (n.d.). EE5390: Analog IC Design [Recorded lecture]. Retrieved from http://www.ee.iitm.ac.in/~ani/ee5390/index.html Page 15 of 69
6. Baker, R. J. (2019). CMOS: Circuit design, layout, and simulation (4th ed.). Wiley IEEE Press.

ONLINE RESOURCES:

3. https://nptel.ac.in/courses/108108111?utm_source=chatgpt.com\
4. https://nptel.ac.in/courses/108102112
5. https://nptel.ac.in/courses/108106105

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain the theory and design concepts of analog circuits .
CO2	Analyze and design single-stage and multi-stage amplifiers considering high-frequency and noise characteristics to meet specified performance criteria.
CO3	Apply concepts of negative feedback, stability, and frequency compensation in the design and analysis of operational amplifiers.
CO4	Design and simulate voltage and current reference circuits with temperature and supply independence for analog integrated systems.

Course Outcomes	**Programme Outcomes / Programme Specific Outcomes (POs/PSOs)**				
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO1	-	-	-	-	-
CO2	3	-	-	2	2
CO3	3	3	-	3	3
CO4	3	3		2	2
Average	2.25	1.5	0	1.75	1.75

1. Low 2. Medium 3. High

26VLC07L	**Analog IC Design Laboratory**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

COURSE OBJECTIVES:

To Design analog circuits from transistor level to IA implementation using CAD tools for simulation, layout, LVS, and parasitic extraction.

LIST OF EXPERIMENTS:

1. Extraction of process parameters of CMOS process transistors

a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.

b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt.

c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and sub- threshold slope.

d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.

e. Extract V^{th} of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract V^{th} use the following procedure.

i. Plot gm vs VGS using SPICE and obtain peak gm point.

ii. Plot y=ID/(gm) as a function of VGS using SPICE.

iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.

f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.

2. CMOS inverter design and performance analysis

a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g.

Calculate VIL, VIH, NMH, NML for the inverter.

ii. Plot VTC for CMOS inverter with varying VDD.

iii. Plot VTC for CMOS inverter with varying device ratio.

b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to- 20% fall time tf.

c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis

a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.

b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.

i. Establish a test bench to achieve VDSQ=VDD/2.
ii. Calculate input bias voltage for a given bias current.
iii. Use spice and obtain the bias current. Compare with the theoretical value
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
v. using small signal analysis in spice, considering load capacitance.
vi. Plot step response of the amplifier with a specific input pulse amplitude.
vii. Derive time constant of the output and compare it with the time constant
viii. Resulted from -3dB Band Width. ix. Use spice to determine input voltage range of the amplifier

5. Three OP AMP Instrumentation Amplifier (INA). Use proper values of resistors to get a three OPAMP INA with differential mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

I. Draw the schematic of op-amp macro model.
II. Draw the schematic of INA.
III. Obtain parameters of the op-amp macro model such that it meets a given specification for:
    i. low-frequency voltage gain,
    ii. unity gain BW (fu),
    iii. input capacitance,
    iv. output resistance,
    v. CMRR a. Draw schematic diagram of CMRR simulation setup.

b. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

c. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

d. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6.Use Layout editor.

a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.

b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.

c. Extract the netlist. Use extracted netlist and obtain tPHLtPLH for the inverter using Spice.

d. Use a specific interconnect length and connect and connect three inverters in a chain.

e. Extract the new netlist and obtain tPHL and tPLH of the middle inverter.

f. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter

a. low-frequency voltage gain,

b. unity gain BW (fu),

c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.

ii. Perform time domain simulation and verify low frequency gain.

iii. Perform AC analysis and verify.

Weightage: Continuous Assessment: 60%, End Semester Examinations: 40%

Continuous Assessment: Project (30%), Assignment (10%), Practical (30%), Internal Examinations (30%)

COURSE OUTCOMES:

At the end of the course students will be able to

CO1: Characterize MOS transistors and design basic analog building blocks using simulation tools

CO2: Implement and simulate analog circuits through schematic entry, layout design, LVS, and parasitic extraction.

CO3: Design and validate an instrumentation amplifier using a structured analog design flow with CAD tools.

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	3	-	-	2	2
CO2	3	3	-	3	3
CO3	3	3	-	2	2
CO4	-	-	-	-	-
Average	2.25	1.5	0	1.75	1.75

1. Low 2. Medium 3. High

SEMESTER-II



26VL201T	Multi-Core Architecture and ISA Verification	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

To Study single-stage amplifier design, high-frequency/noise characteristics, operational amplifiers, voltage/current reference circuits with practical exercises.

UNIT - I	Introduction to Computer Organisation	9 Hours

Computer types , Functional units of a computer , Bus structures, Software, Processor clock, Performance equation, Pipelining and parallel processing, Compiler, Performance measurement, Multiprocessor and Multicomputer.

UNIT - II	Processor	9 Hours

CPU core architecture, Logic design conventions, Datapath, Pipelining Datapath and control, Data and control hazards, Exceptions, Single core to Multi-core architectures, SIMD and MIMD systems , ARM cortex A53 and Intel core i7 pipelines, Qualcomm Snapdragon 888 SoC .

UNIT - III	Instruction Set Architecture	9 Hours

RISC-V Instructions, Base, Single and Double precision floating point, Atomic, Compute instructions – Instruction set representation, Parallel Program Design.

UNIT - IV	Memory Organisation	9 Hours

Memory hierarchy, Types of Memory, SRAM, DRAM, Flash memory, Disk, Cache memory, Cache hit and miss, Cache mapping, Direct mapping, Associative mapping and Set-associative mapping , DDR4 RAM.

UNIT - V	ISA Verification	9 Hours

Decimal to floating point converter design, Floating point arithmetic modules design and verification, OP-Code generation for integer, floating point, atomic, compressed instructions set.

Total Hours	45

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

REFERENCES :

1. David Patterson and John. L. Hennessy – Computer Organization and Design (The hardware/software interface RISC-V Edition) Elsevier, 2018..
2. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization",. Tata McGraw Hill, Fifth Edition, 2002
3. Peter S. Pacheco, —An Introduction to Parallel Programming, MorganKauffman/Elsevier, 2011
4. Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanović, "The RISC-V Instruction Set

Manual, Volume I: User-Level ISA Version 2.1", Technical Report UCB/EECS-2016-118, EECS Department, University of California, Berkeley, May 31, 2016

5. Andrew Waterman, Yunsup Lee, Rimas Avižienis, David A. Patterson, and Krste Asanović, "The RISC-V Instruction Set Manual, Volume II: Privileged Architecture Version 1.9", Technical Report UCB/EECS-2016-129, EECS Department, University of California, Berkeley, July 8, 2016 .

ONLINE RESOURCES:

1. https://nptel.ac.in/courses/108108111?utm_source=chatgpt.com\
2. https://nptel.ac.in/courses/108102112
3. https://nptel.ac.in/courses/108106105

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain computer organization, functional units, pipelining, parallel processing, and performance measurement of multi-core systems
CO2	Analyze CPU core architectures, pipeline design, hazards, exceptions, and SIMD/MIMD multi-core systems (ARM Cortex-A53, Intel i7, Snapdragon 888)
CO3	Apply instruction set architecture (RISC-V) concepts including base, floating-point, atomic, and compute instructions for parallel program design
CO4	Design and verify ISA modules including decimal-to-floating point converters, floating point arithmetic modules, and opcode generation for integer, floating point, atomic, and compressed instructions

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO1	-	-	-	-	-
CO2	3	2	3	2	2
CO3	3	2	3	2	3
CO4	3	2	3	3	3
Average	2	2	2	2	2

1. Low **2. Medium** **3. High**

26VL202T	Data Converters IC Design	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

To provide a comprehensive understanding of analog-to-digital and digital-to-analog converter architectures, focusing on the fundamental principles of sampling, quantization, oversampling, and switched-capacitor circuit design.

UNIT - I	Introduction & Characteristics of AD/DA Converter Characteristics	9 Hours

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and anti-aliasing filters.

UNIT - II	Switch Capacitor Circuits and Comparators	9 Hours

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques.

UNIT - III	Nyquist Rate D/A Converters	9 Hours

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

UNIT - IV	Pipeline And Other ADCs	9 Hours

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT - V	Sigma Delta Converters	9 Hours

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities

Total Hours	45

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. "Analysis and Design of Data Converters" — Behzad Razavi (Cambridge University Press, 2025)
2. "Advanced Tutorial on Analog Circuit Design" — Milin Zhang, Zhihua Wang, Jan Van Der Spiegel, and Franco Maloberti (River Publishers, 2023).
3. "CMOS Analog and Mixed-Signal Circuit Design: Practices and Innovations" — Jagdish Lal Raheja et al. (Routledge / CRC Press, 2023).

ONLINE COURSES:

1. https://nptel.ac.in/courses/117106034
2. https://www.google.com/search?q=https://archive.nptel.ac.in/courses/117106034/

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain the characteristics, types, and applications of ADCs and DACs, including sampling, quantization, reconstruction, oversampling, and anti-aliasing
CO2	Analyze switched-capacitor circuits and comparators, including offset cancellation and calibration techniques.
CO3	Apply Nyquist-rate DAC and ADC design concepts including current-steering DACs, binary vs thermometer DACs, DNL, INL, and zero-order hold circuits
CO4	Design and evaluate pipeline, flash, successive approximation, time-interleaved, and sigmadelta ADC architectures with performance metrics and modulator characteristics

Course Outcomes	**Programme Outcomes / Programme Specific Outcomes (POs/PSOs)**				
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO1	-	-	-	-	-
CO2	2	2	-	2	2
CO3	3	2	2	3	3
CO4	3	3	2	2	2
Average	2	1.75	1	2	1.75

2. Low **2. Medium** **3. High**

VL25203	**VLSI Testing and Verification Using UVM**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce the VLSI testing, logic and fault simulation and testability measures. To study the test generation for combinational and sequential circuit and to to provide the students complete understanding on UVM testing. To become proficient at UVM verification

UNIT - I	**Introduction to VLSI Testing**	**9 Hours**

Introduction - VLSI Testing Process and Test Equipment- Challenges in VLSI Testing - Test Economics and Product Quality- Fault Modelling - Relationship among Fault Models.

UNIT - II	**Logic & Fault Simulation & Testability Measures**	**9 Hours**

Simulation for Design Verification and Test Evaluation - Modelling Circuits for Simulation - Algorithms for True Value and Fault Simulation - Scoap Controllability and observability

UNIT - III	**Test Generation for Combinational and Sequential Circuits**	**9 Hours**

Algorithms and Representations - Redundancy Identification - Combinational ATPG Algorithms - Sequential ATPG Algorithms - Simulation Based ATPG - Genetic Algorithm Based ATPG		
UNIT - IV	**Introduction to UVM**	**9 Hours**
Overview- The Typical UVM Test bench Architecture- The UVM Class Library Transaction-Level Modelling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation		
UNIT - V	**Developing Reusable Verification Components**	**9 Hours**
Modelling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage .		
	Total Hours	**45**

Activities :

- Do microcontroller based design experiments.
- Create program -state models for different embedded applications.
- Design and develop embedded solutions for real world problems

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017
2. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press

ONLINE RESOURCES:

1. https://nptel.ac.in/courses/106103016
2. https://nptel.ac.in/courses/117103125

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain VLSI testing concepts, fault modeling, test economics, and product quality in chip verification
CO2	Analyze logic and fault simulation techniques, controllability/observability measures, and testability of combinational and sequential circuits
CO3	Apply ATPG (Automatic Test Pattern Generation) algorithms, including combinational, sequential, simulation-based, and GA-based test pattern generation
CO4	Design and implement reusable UVM verification components using TLM, agents, drivers, sequencers, monitors, environments, and test scenarios

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	-	-	-	-	-
CO2	-	3	3	3	2
CO3	1	1	3	3	3
CO4	1	-	3	2	3
Average	1	2	3	2.67	2.67

3. Low 2. Medium 3. High

VL25204	Low Power VLSI Design	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To know the low power low voltage VLSI design. understand the impact of power on system performances and know about different Design approaches. Identify suitable techniques to reduce power dissipation in combinational and sequential circuits. Understand the design of low power memories

UNIT - I	Fundamentals	9 Hours

Need for Low Power Circuit Design, Sources of Power Dissipation - Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects - Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact lornization, Hot Electron Effect.

UNIT - II	Low-Power Design Approaches	9 Hours

Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach -Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures

UNIT - III	Low-Voltage Low-Power Adders	9 Hours

Introduction, Standard Adder Cells, CMOS Adder's Architectures - Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low Voltage Low-Power Design Techniques - Trends of Technology and Power Supply Voltage, Low Voltage Low-Power Logic Styles.

UNIT - IV	Low-Voltage Low-Power Multipliers	9 Hours

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V	Low-Voltage Low-Power Memories	9 Hours
Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre charge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.		
	Total Hours	**45**

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis and Design", TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.
3. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Page 27 of 69 Perspective", CRC Press
4. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press, /Wiley International, 1998.
5. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley, & Sons, 2000.
6. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
7. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", A Kluwer Academic Press.
8. Siva G. Narendran, Anatha Chandrakasan, "Leakage in Nanometer CMOS Technologies", Springer, 2005.

ONLINE RESOURCES:

1. https://nptel.ac.in/courses/106105034
2. https://nptel.ac.in/courses/106105161

COURSE OUTCOME:

After successful completion of this course, the students shall be able to

CO1	Explain the fundamentals of low-power VLSI design, sources of power dissipation, and short channel effects
CO2	Analyze and apply low-power design approaches at circuit and architectural levels, including voltage scaling, VTCMOS/MTCMOS, and switched-capacitance minimization
CO3	Design low-voltage low-power arithmetic circuits: adders and multipliers using Ripple Carry, Carry Look-Ahead, Carry Select, Braun, Baugh Wooley, Booth, and Wallace Tree architectures
CO4	Design and evaluate low-power memories: ROM, SRAM, and DRAM using low-power techniques, pre charge/equalization circuits, and self-refresh mechanisms

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	-	-	-	-	-
CO2	3	3	3	3	3
CO3	2	3	1	3	3
CO4	3	2	3	2	3
Average	2	2	1.75	2	2.25

1. Low 2. Medium 3. High

26VL206L	VERIFICATION USING UVM LABORATORY	L	T	P	C
		0	0	4	2

COURSE OBJECTIVES:

To help the engineers to design the system with verilog and system verilog • Complete understanding of Verilog Hardware Description Language , to practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

LIST OF EXPERIMENTS:

1. Simulate a simple UVM test bench and DUT.
2. Examining the UVM test bench.
3. Design and simulate sequence items and sequence.
4. Design and simulate a UVM driver and sequencer.
5. Design and simulating UVM monitor and agent.
6. Design, simulate and examine coverage.
7. Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT.
8. Design and simulate a test that runs multiple sequence.
9. Design and simulate a configurable UVM test environment.

Weightage: Continuous Assessment: 60%, End Semester Examinations: 40%

Continuous Assessment: Project (30%), Assignment (10%), Practical (30%), Internal Examinations (30%)

COURSE OUTCOMES:

At the end of the course students will be able to

CO1: Apply Verilog and System Verilog for designing and simulating digital systems

CO2: Develop and simulate UVM testbenches including sequence items, drivers, sequencers, monitors, and agents

CO3: Implement verification components such as coverage, scoreboard, and configurable UVM environments.

CO4: Analyze and verify DUT functionality using UVM environment and multiple test sequences.

Course Outcomes	Programme Outcomes / Programme Specific Outcomes (POs/PSOs)				
	PO1	PO2	PO3	PSO1	PSO2
CO1	-	-	-	-	-
CO2	3	3	2	3	2
CO3	3	3	2	3	2
CO4	3	3	2	3	3
Average	2.25	2.25	1.5	2.25	1.75

1.Low 2. Medium 3. High

